Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (currently amended): Instruction Set Architecture (ISA) selection logic within a CPU for selecting an ISA decoding mode for a program instruction from a plurality of ISA decoding modes, the program instruction retrieved from an address in an address space of the CPU, the selection logic comprising:

a plurality of boundary address registers for storing boundary addresses that partition the address space into a plurality of address ranges corresponding to the plurality of ISA decoding modes, wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA decoding mode; and

ISA mode selection logic, coupled to said plurality of boundary address registers, for receiving the address, and for comparing the address to said boundary addresses to determine the ISA decoding mode for the program instruction.

Claim 2 (original): The selection logic as recited in claim 1, wherein the CPU executes a multiple-ISA application program.

Claim 3 (previously presented): The selection logic as recited in claim 2, wherein said multiple-ISA application program comprises program components having program instructions corresponding to said plurality of ISA decoding modes.

Claim 4 (original): The selection logic as recited in claim 3, wherein said program instructions that correspond to a first ISA decoding mode are located within a first one of said plurality of address ranges.

Claim 5 (original): The selection logic as recited in claim 1, wherein each of said plurality of boundary address registers stores a boundary address for a corresponding address range.

Claim 6 (original): The selection logic as recited in claim 5, wherein said boundary address comprises a lower address boundary for said corresponding one of said plurality of address ranges.

Claim 7 (original): The selection logic as recited in claim 6, wherein said ISA mode selection logic determines that a particular boundary address register corresponds to one of said plurality of address ranges within which said address is located.

Claim 8 (original): The selection logic as recited in claim 7, wherein said ISA mode selection logic selects the ISA decoding mode corresponding to said particular boundary address register.

Claim 9 (original): The selection logic as recited in claim 8, wherein said ISA mode selection logic provides the ISA decoding mode to instruction decoding logic to enable correct decoding of the program instruction.

Claim 10 (currently amended): An Instruction Set Architecture (ISA) mode selection apparatus in a CPU, comprising:

decoding logic, for decoding a program instruction retrieved from an address within an address space of the CPU;

a boundary address register file, for storing boundary addresses that map one or more ISA modes of the CPU to corresponding address ranges within said address space, wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA mode; and

an ISA mode controller, coupled to said boundary address register file, and to said decoding logic, for designating to said decoding logic an ISA mode to be used to decode said program instruction according to said address.

Claim 11 (original): The ISA mode selection apparatus as recited in claim 10, wherein said program instruction is within an application program that comprises components, each of said components having program instructions that correspond to only one of said one or more ISA modes.

Claim 12 (original): The ISA mode selection apparatus as recited in claim 11, wherein first program components corresponding to a first ISA mode are located within a first address range.

Claim 13 (original): The ISA mode selection apparatus as recited in claim 10, wherein said boundary address register file comprises:

a plurality of boundary address registers, each storing one of said boundary addresses.

Claim 14 (original): The ISA mode selection apparatus as recited in claim 13, wherein said boundary addresses comprise lower address boundaries for said corresponding address ranges.

Claim 15 (original): The ISA mode selection apparatus as recited in claim 14, wherein said ISA mode controller comprises address evaluation logic for determining which one of said plurality of boundary address registers corresponds to said program instruction.

Claim 16 (original): The ISA mode selection apparatus as recited in claim 15, wherein said ISA mode controller designates to said decoding logic said ISA mode based upon determining which one of said plurality of boundary address registers corresponds to the program instruction.

Claim 17 (original): The ISA mode selection apparatus as recited in claim 10, wherein said ISA mode controller provides said ISA mode to said decoding logic to enable correct processing of said program instruction.

Claim 18 (currently amended): A CPU for executing a multiple-ISA program, comprising:

ISA mode selection logic, configured to provide a first ISA mode indicator that corresponds to a first program instruction, said first program instruction being fetched from a first address in memory;

ISA mode boundary address registers, coupled to said ISA mode selection logic, configured to store boundary addresses that partition said memory into address ranges, wherein a plurality of ISA modes is mapped to said address ranges, and wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA mode; and

an instruction decoder, coupled to said ISA mode selection logic, configured to receive said first ISA mode indicator, and configured to decode said first instruction according to said first ISA mode.

Claim 19 (original): The CPU as recited in claim 18, wherein the multiple-ISA program comprises components that are stored within a corresponding address range.

Claim 20 (original): The CPU as recited in claim 18, wherein said ISA mode boundary address registers contain said boundary addresses that designate said address ranges.

Claim 21 (original): The CPU as recited in claim 20, wherein said boundary addresses comprise lower address boundaries for said address ranges.

Claim 22 (previously presented): The CPU as recited in claim 21, wherein said ISA mode selection logic determines which one of said ISA mode boundary address registers corresponds to said first address.

Claim 23 (original): The CPU as recited in claim 22, wherein said ISA mode selection logic provides said first ISA mode indicator to said instruction decoder to enable correct processing of said first program instruction.

Claim 24 (currently amended): A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a CPU to be described, said CPU for executing a multiple-ISA application program, said computer readable program code comprising:

first program code, for providing boundary address registers, configured to partition an address space of said CPU into address ranges, said address ranges corresponding to associated ISA modes, wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA mode; and

second program code, for providing ISA mode selection logic, configured to receive an address from which a program instruction was retrieved, and configured to compare said address against said address ranges to determine an ISA mode for processing said program instruction.

Claim 25 (original): The computer program product as recited in claim 24, wherein said multiple-ISA application program comprises program components corresponding to said associated ISA modes.

Claim 26 (original): The computer program product as recited in claim 25, wherein each of said boundary address registers contains an address boundary for a corresponding address range.

Claim 27 (original): The computer program product as recited in claim 26, wherein said address boundary comprises a lower address boundary for said corresponding address range.

Claim 28 (original): The computer program product as recited in claim 27, wherein said ISA mode selection logic determines a particular boundary address register that corresponds to said address.

Claim 29 (original): The computer program product as recited in claim 28, wherein said ISA mode selection logic determines said ISA mode that corresponds to said particular boundary address register.

Claim 30 (currently amended): A method in a CPU for selecting an Instruction Set Architecture (ISA) mode during execution of an application program, the application program having program instructions according to a plurality of ISA modes, the method comprising:

a) partitioning an address space of the CPU into address ranges, the address ranges being designated by contents of a boundary register file, wherein the size of an address range corresponds to the distribution of program instructions for a corresponding ISA mode;

b) mapping each of the address ranges to each of the plurality of ISA modes; and

c) selecting the ISA mode for processing of [[the]] a program instruction according to said mapping.

Claim 31 (original): The method as recited in claim 30, wherein said partitioning comprises:

i) specifying address boundaries within registers in the boundary register file.

Claim 32 (original): The method as recited in claim 30, wherein said mapping comprises:

i) storing individual components of the application program within an associated address range that is designated for processing of program instructions corresponding to an associated ISA mode.

Claim 33 (original): The method as recited in claim 32, wherein said mapping further comprises:

ii) evaluating an address of a program instruction fetched during execution of the application program against the contents of the boundary register file to determine a particular address range within which the program instruction lies.

Claim 34 (currently amended): A computer data signal embodied in a transmission medium, comprising:

first computer-readable program code, for providing boundary address registers, said registers being configured to partition an address space into address ranges, said address ranges corresponding to associated ISA modes, wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA mode.

Claim 35 (original): The computer data signal as recited in claim 34, further comprising:

second computer-readable program code, for providing ISA mode selection logic, said ISA mode selection logic being configured to receive an address associated with a program instruction, and configured to compare said address against said address ranges to determine an ISA mode for processing said program instruction.